NE5534x, SA5534x Low-Noise Operational Amplifiers

1 Features

- Equivalent Input Noise Voltage 3.5 nV/√Hz Typ
- Unity-Gain Bandwidth 10 MHz Typ
- Common-Mode Rejection Ratio 100 dB Typ
- High DC Voltage Gain 100 V/mV Typ
- Peak-to-Peak Output Voltage Swing 32 V Typ With $V_{CC\pm}$ = ±18 V and R_L = 600 Ω
- High Slew Rate 13 V/μs Typ
- Wide Supply-Voltage Range ±3 V to ±20 V
- Low Harmonic Distortion
- Offset Nulling Capability
- External Compensation Capability

2 Applications

- Audio Preamplifiers
- Servo Error Amplifiers
- Medical Equipment
- Telephone Channel Amplifiers

3 Description

The NE5534, NE5534A, SA5534, and SA5534A devices are high-performance operational amplifiers combining excellent dc and ac characteristics. Some of the features include very low noise, high output-drive capability, high unity-gain and maximum-output-swing bandwidths, low distortion, and high slew rate.

These operational amplifiers are compensated internally for a gain equal to or greater than three. Optimization of the frequency response for various applications can be obtained by use of an external compensation capacitor between COMP and COMP/BAL. The devices feature input-protection diodes, output short-circuit protection, and offset-voltage nulling capability with use of the BALANCE and COMP/BAL pins (see Figure 10).

For the NE5534A and SA5534A devices, a maximum limit is specified for the equivalent input noise voltage.

Device Information

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
NE5534x	SOIC (8)	4.90 mm × 3.91 mm
SA5534x	SOIC (8)	4.90 mm × 3.91 mm
	SO (8)	6.20 mm × 5.30 mm

4 Simplified Schematic

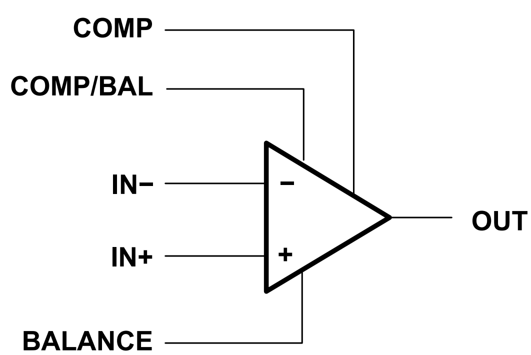


Table of Contents

1 Features 1
2 Applications 1
3 Description 1
4 Simplified Schematic 1
5 Revision History 2
6 Pin Configuration and Functions 3
7 Specifications 4
7.1 Absolute Maximum Ratings 4
7.2 Handling Ratings 4
7.3 Recommended Operating Conditions 4
7.4 Thermal Information 4
7.5 Electrical Characteristics 5
7.6 Operating Characteristics 6
7.7 Typical Characteristics 7
8 Detailed Description 9
8.1 Overview 9
8.2 Functional Block Diagram 9
8.3 Feature Description 10
8.4 Device Functional Modes 10
9 Application and Implementation 11
9.1 General Application 11
9.2 Typical Application 12
10 Power Supply Recommendations 14
11 Layout 15
11.1 Layout Guidelines 15
11.2 Layout Example 15
12 Device and Documentation Support 16
12.1 Related Links 16
12.2 Trademarks 16
12.3 Electrostatic Discharge Caution 16
12.4 Glossary 16
13 Mechanical, Packaging, and Orderable Information 16

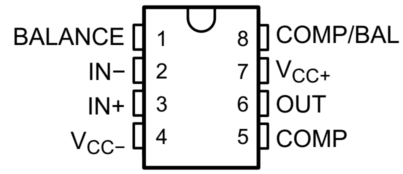
5 Revision History

Changes from Revision C (September 2004) to Revision D **Page**

- Added *Applications*,*Device Information* table, *Handling Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
- Deleted *Ordering Information* table. 1

6 Pin Configuration and Functions

NE5534, SA5534 . . . D (SOIC), P (PDIP), OR PS (SOP) PACKAGE
NE5534A, SA5534A . . . D (SOIC) OR P (PDIP) PACKAGE
(TOP VIEW)



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
BALANCE	1	I	External frequency compensation
COMP/BAL	8	I	External offset voltage adjustment/External frequency compensation
COMP	5	O	External offset voltage adjustment
IN+	3	I	Noninverting input
IN-	2	I	Inverting Input
OUT	6	O	Output
V_{CC+}	7	—	Positive Supply
V_{CC-}	4	—	Negative Supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage(2)	V_{CC+}	0		22	V
		$V_{CC–}$	–22		0	V
	Input voltage, either input(2)(3)		$V_{CC–}$		V_{CC+}	V
	Input current(4)		–10		10	mA
	Duration of output short circuit(5)		Unlimited			
T_J	Operating virtual-junction temperature				150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and $V_{CC–}$.
(3) The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
(4) Excessive current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs, unless some limiting resistance is used.
(5) The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	0	200	

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage	V_{CC+}	5	15	V
		$V_{CC–}$	–5	–15	V
T_A	Operating free-air temperature	NE5534, NE5534A	0	70	°C
		SA5534, SA5534A	–40	85	

7.4 Thermal Information

THERMAL METRIC(1)		NE5534, NE5534A SA5534, and SA5534A			UNIT
		D	P	PS	
		8 PINS			
$R_{θJA}$	Package thermal impedance(2)(3)	97	85	95	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).
(2) The package thermal impedance is calculated in accordance with JESD 51-7.
(3) Maximum power dissipation is a function of T_J(max), $θ_{JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A) / θ_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

7.5 Electrical Characteristics

$V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0 R_S = 50 Ω	T_A = 25°C		0.5	4	mV
			T_A = Full range			5	
I_{IO}	Input offset current	V_O = 0	T_A = 25°C		20	300	nA
			T_A = Full range			400	
I_{IB}	Input bias current	V_O = 0	T_A = 25°C		500	1500	nA
			T_A = Full range			2000	
V_{ICR}	Common-mode input-voltage range			±12	±13		V
$V_{O(PP)}$	Maximum peak-to-peak output-voltage swing	R_L ≥ 600 Ω	$V_{CC\pm}$ = ±15 V	24	26		V
			$V_{CC\pm}$ = ±18 V	30	32		
A_{VD}	Large-signal differential-voltage amplification	V_O = ±10 V R_L ≥ 600 Ω,	T_A = 25°C	25	100		V/mV
			T_A = Full range	15			
		R_L ≥ 2 kΩ, V_O±10 V	T_A = 25°C	25	100		
			T_A = Full range	15			
A_{vd}	Small-signal differential-voltage amplification	f = 10 kHz	C_C = 0		6		V/mV
			C_C = 22 pF		2.2		
B_{OM}	Maximum output-swing bandwidth	V_O = ±10 V	C_C = 0		200		kHz
			C_C = 22 pF		95		
		$V_{CC\pm}$ 18 V, R_L = 600 Ω	V_O = ±14 V C_C = 22 pF		70		
B_1	Unity-gain bandwidth	C_C = 22 pF	C_L = 100 pF		10		MHz
r_i	Input resistance			30	100		kΩ
z_o	Output impedance	A_{VD} = 30 dB, C_C = 22 pF	R_L = 600 Ω, f = 10 kHz		0.3		Ω
CMRR	Common-mode rejection ratio	V_O = 0, R_S = 50 Ω	V_{IC} = V_{ICR}min	70	100		dB
k_{SVR}	Supply-voltage rejection ratio (ΔV_{CC} or ΔV_{IO})	$V_{CC\pm}$ = ±9 V to ±15 V, V_O = 0	R_S = 50 Ω	80	100		dB
I_{OS}	Output short-circuit current				38		mA
I_{CC}	Total supply current	V_O = 0, No load	T_A = 25°C		4	8	mA

(1) All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified. For NE5534 and NE5534A, full range is 0°C to 70°C. For SA5534 and SA5534A, full range is –40°C to 85°C.

7.6 Operating Characteristics

$V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		NE5534, SA5534	NE5534A, SA5534A			UNIT
					TYP	MIN	TYP	MAX	
SR	Slew rate		C_C = 0		13		13		V/µs
			C_C = 22 pF		6		6		
t_r		Rise time	V_I = 50 mV, R_L = 600 Ω, C_L = 100 pF	A_{VD} = 1, C_C = 22 pF	20		20		ns
		Overshoot factor			20		20		%
		Rise time	V_I = 50 mV, R_L = 600 Ω, C_L = 500 pF	A_{VD} = 1, C_C = 47 pF	50		50		ns
		Overshoot factor			35%		35%		—
V_n	Equivalent input noise voltage		f = 30 Hz		7		5.5	7	nV/√Hz
			f = 1 kHz		4		3.5	4.5	
I_n	Equivalent input noise current		f = 30 Hz		2.5		1.5		pA/√Hz
			f = 1 kHz		0.6		0.4		
$\overline{F}$	Average noise figure		R_S = 5 kΩ	f = 10Hz to 20 kHz			0.9		dB

7.7 Typical Characteristics

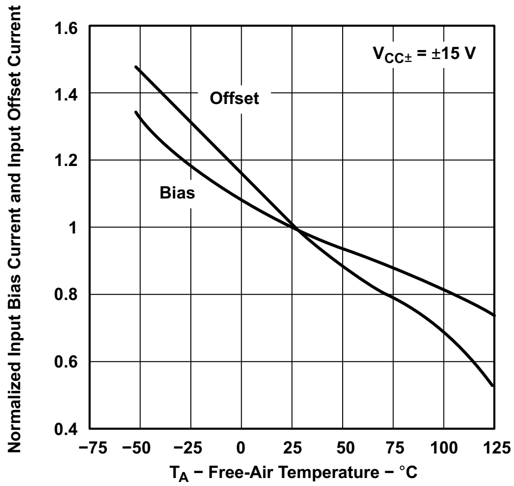


Figure 1. Normalized Input Bias Current and Input Offset Current vs Free-Air Temperature

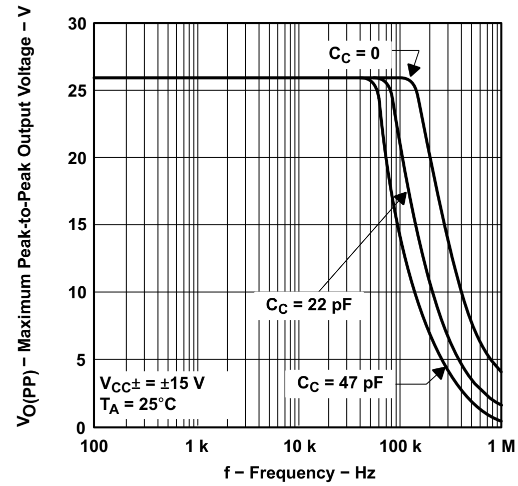


Figure 2. Maximum Peak-to-Peak Output Voltage vs Frequency

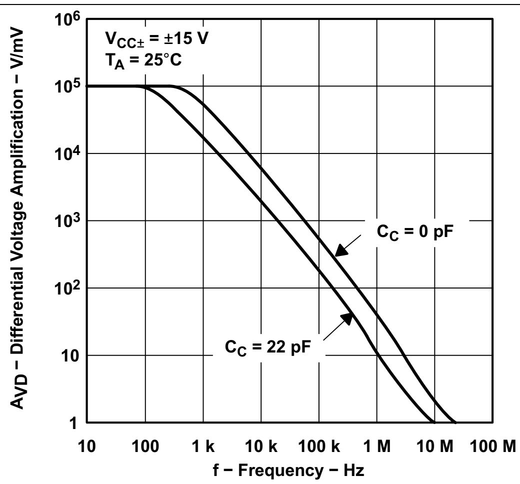


Figure 3. Large-Signal Differential Voltage Amplification vs Frequency

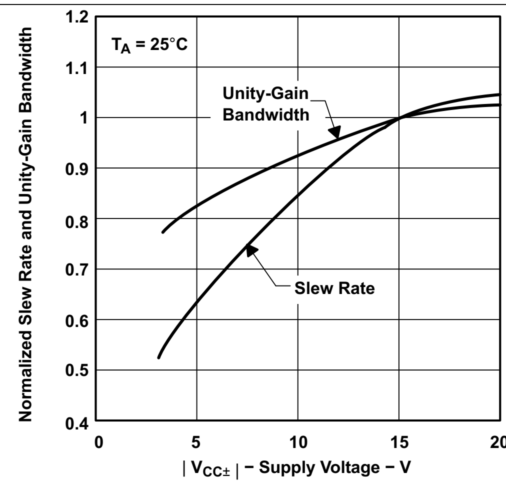


Figure 4. Normalized Slew Rate and Unity-Gain Bandwidth vs Supply Voltage

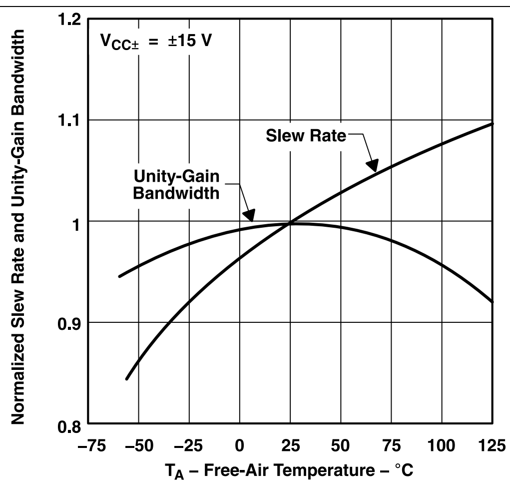


Figure 5. Normalized Slew Rate and Unity-Gain Bandwidth vs Free-Air Temperature

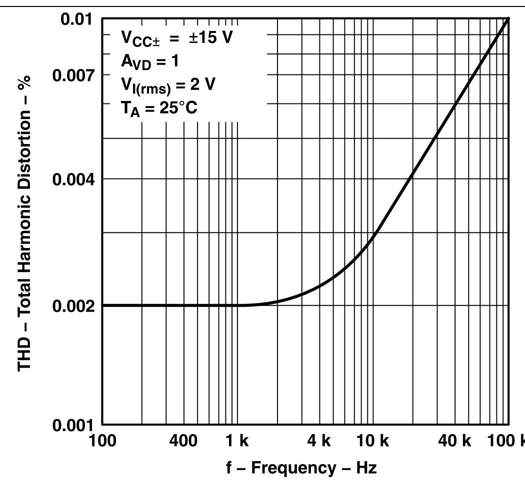


Figure 6. Total Harmonic Distortion vs Frequency

Typical Characteristics (continued)

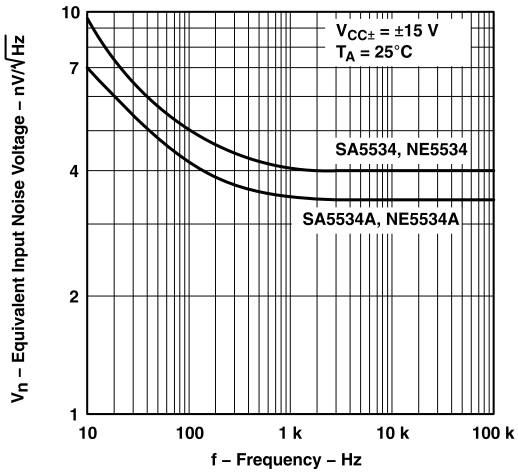


Figure 7. Equivalent Input Noise Voltage vs Frequency

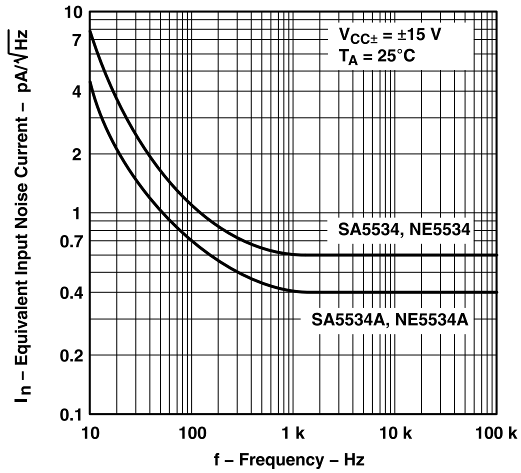


Figure 8. Equivalent Input Noise Current vs Frequency

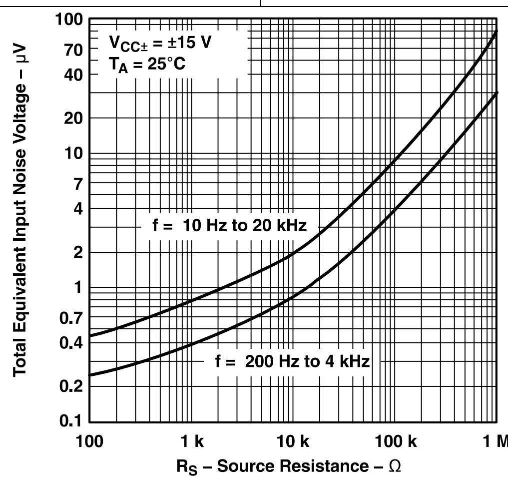


Figure 9. Total Equivalent Input Noise Voltage vs Source Resistance

8 Detailed Description

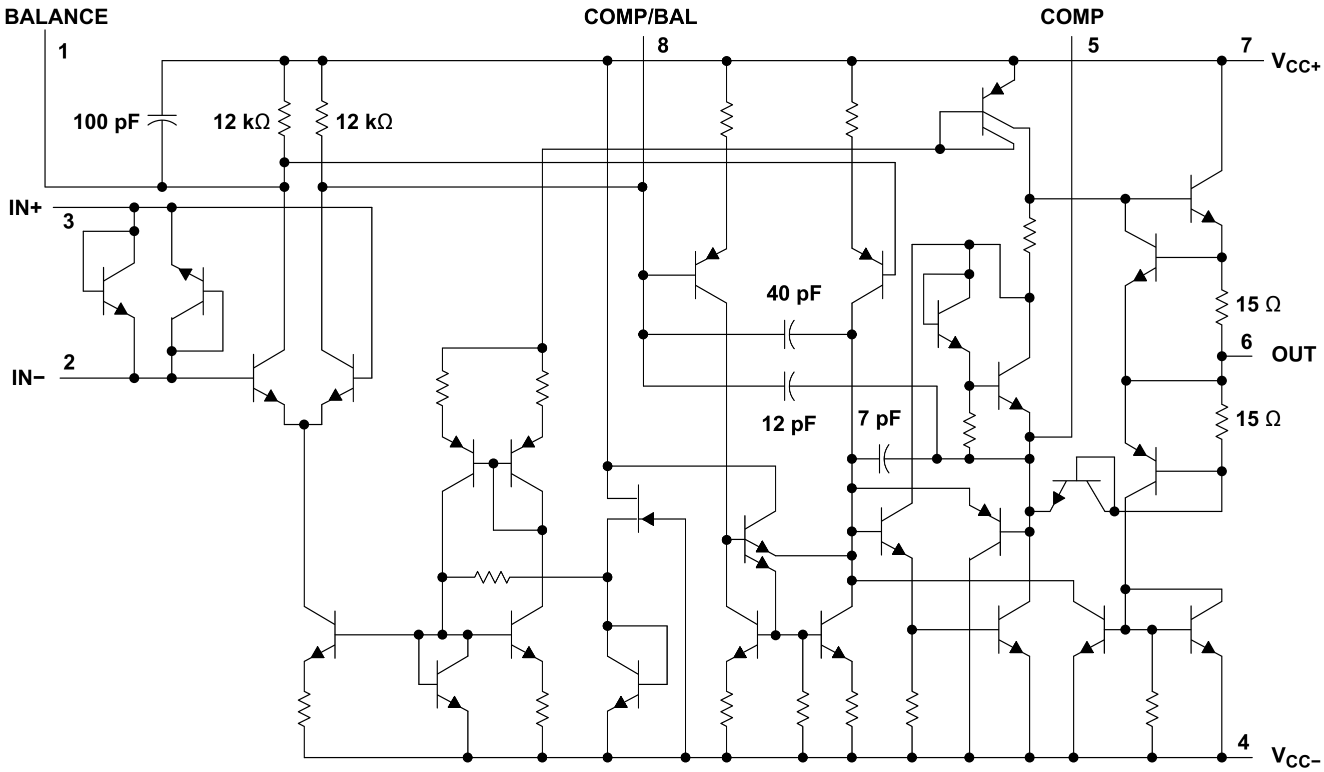
8.1 Overview

The NE5534, NE5534A, SA5534, and SA5534A devices are high-performance operational amplifiers combining excellent dc and ac characteristics. Some of the features include very low noise, high output-drive capability, high unity-gain and maximum-output-swing bandwidths, low distortion, and high slew rate.

These operational amplifiers are compensated internally for a gain equal to or greater than three. Optimization of the frequency response for various applications can be obtained by use of an external compensation capacitor between COMP and COMP/BAL. The devices feature input-protection diodes, output short-circuit protection, and offset-voltage nulling capability with use of the BALANCE and COMP/BAL pins (see the *Application Circuit Diagram*).

For the NE5534A and SA5534A devices, a maximum limit is specified for the equivalent input noise voltage.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Offset-Voltage Null Capability

The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain betas (β), collector or emitter resistors, and so on. The input offset pins allow the designer to adjust for these mismatches by external circuitry. See the *Application and Implementation* section for more details on design techniques.

8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. The NE5534 and SA5534 devices have a 13-V/μs slew rate.

8.3.3 Common-Mode Rejection Ratio

The common-mode rejection ratio (CMRR) of an amplifier is a measure of how well the device rejects unwanted input signals common to both input leads. It is found by taking the ratio of the change in input offset voltage to the change in the input voltage and converting to decibels. Ideally the CMRR is infinite, but in practice, amplifiers are designed to have it as high as possible. The CMRR of the NE5534 and SA5534 devices is 100 dB.

8.3.4 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. The NE5534 and SA5534 devices have a 10-MHz unity-gain bandwidth.

8.3.5 External Compensation Capability

Frequency compensation with a capacitor may be used to increase the gain-bandwidth product (GBW) of the amplifier. See the *Application and Implementation* section for more details on design techniques.

8.4 Device Functional Modes

The NE5534 and SA5534 devices are powered on when the supply is connected. Each of these devices can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

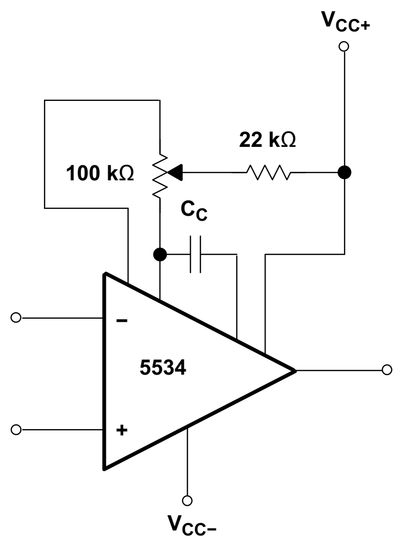
9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 General Application

The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain betas (β), collector or emitter resistors, and so on. The input offset pins allow the designer to adjust for these mismatches by external circuitry. These input mismatches can be adjusted by putting resistors or a potentiometer between the inputs as shown in Figure 10. A potentiometer can be used to fine tune the circuit during testing or for applications which require precision offset control. More information about designing using the input-offset pins, see *Offset Voltage of Operational Amplifiers* (SLOA045).



Frequency Compensation and Offset-Voltage Nulling Circuit

Figure 10. Application Circuit

9.2 Typical Application

The voltage follower configuration of the operational amplifier is used for applications where a weak signal is used to drive a relatively high current load. This circuit is also called a buffer amplifier or unity gain amplifier. The inputs of an operational amplifier have a very high resistance which puts a negligible current load on the voltage source. The output resistance of the operational amplifier is almost negligible, so it can provide as much current as necessary to the output load.

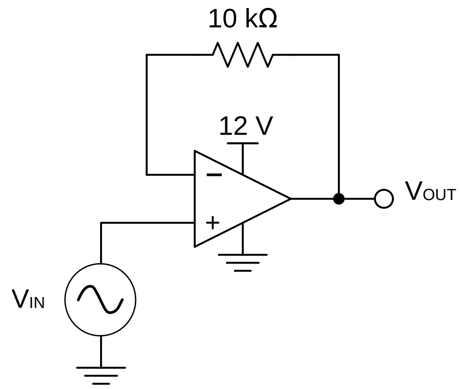


Figure 11. Voltage Follower Schematic

9.2.1 Design Requirements

- Output range of 2 V to 11 V
- Input range of 2 V to 11 V

9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Swing

The output voltage of an operational amplifier is limited by its internal circuitry to some level below the supply rails. For this amplifier, the output voltage swing is within ±12 V, which accommodates the input and output voltage requirements.

9.2.2.2 Supply and Input Voltage

For correct operation of the amplifier, neither input must be higher than the recommended positive supply rail voltage or lower than the recommended negative supply rail voltage. The chosen amplifier must be able to operate at the supply voltage that accommodates the inputs. Because the input for this application goes up to 11 V, the supply voltage must be 12 V. Using a negative voltage on the lower rail rather than ground, allows the amplifier to maintain linearity for inputs below 2 V.

Typical Application (continued)

9.2.3 Application Curves for Output Characteristics

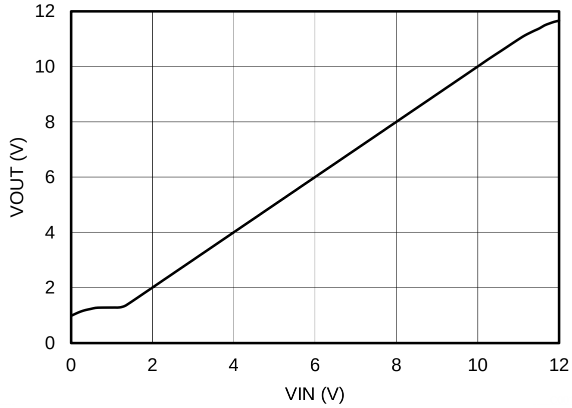


Figure 12. Output Voltage vs Input Voltage

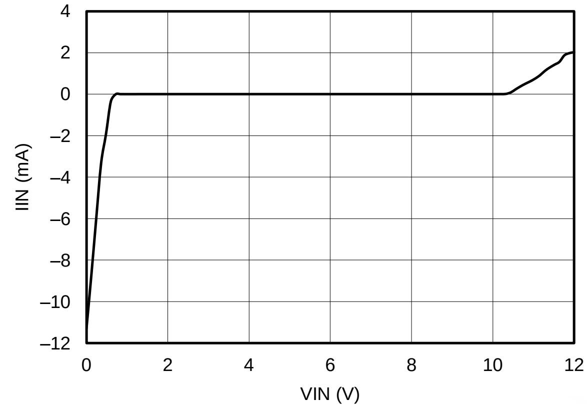


Figure 13. Current Drawn by the Input of the Voltage Follower (I_{IN}) vs the Input Voltage

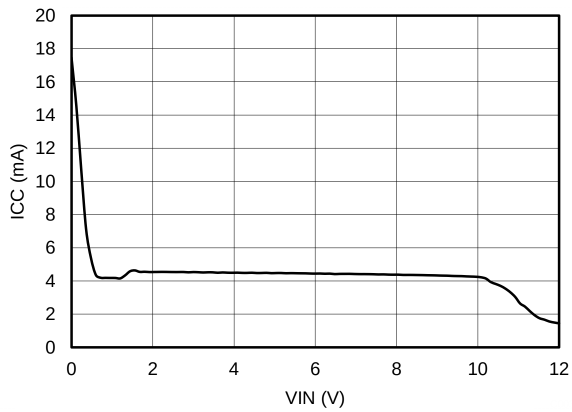


Figure 14. Current Drawn from Supply (I_{CC}) vs the Input Voltage

10 Power Supply Recommendations

The NE5534 and SA5534 devices are specified for operation from ±5 to ±15 V; many specifications apply from 0°C to 70°C for the NE5534 device and –40°C to 85°C for the SA5534 device.

CAUTION

Supply voltages larger than ±22 V can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines*.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. On multilayer PCBs, one or more layers are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques* (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicularly, as opposed to in parallel, with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in .
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

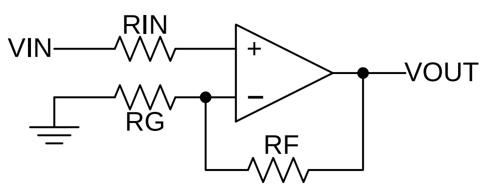


Figure 15. Operational Amplifier Schematic for Noninverting Configuration

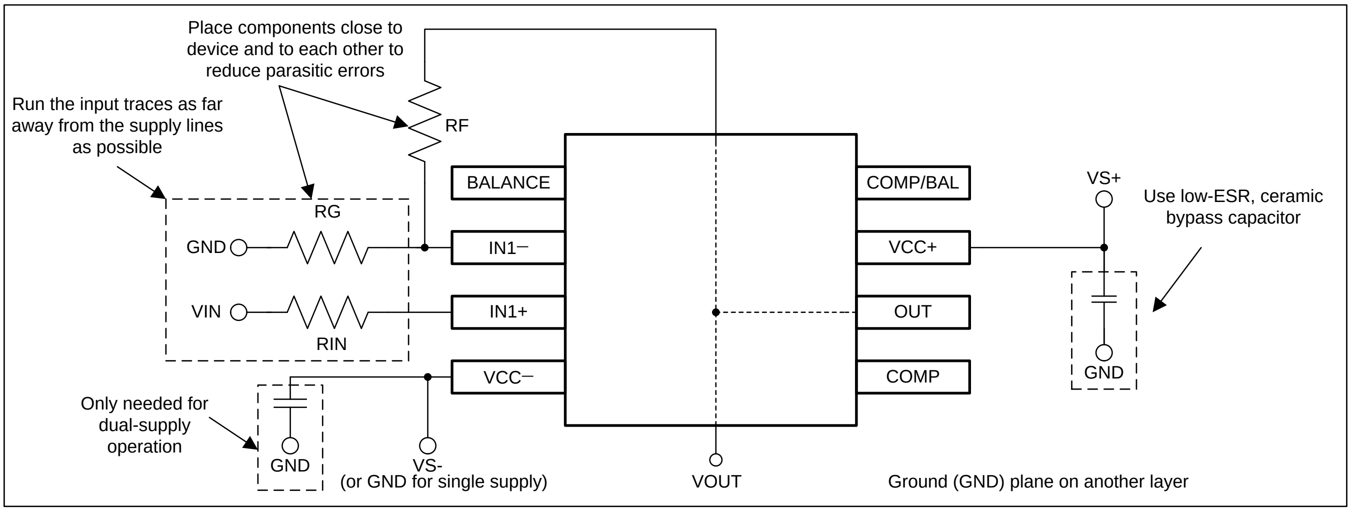


Figure 16. Operational Amplifier Board Layout for Noninverting Configuration

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
NE5534	Click here	Click here	Click here	Click here	Click here
NE5534A	Click here	Click here	Click here	Click here	Click here
SA5534	Click here	Click here	Click here	Click here	Click here
SA5534A	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
NE5534AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	5534A	Samples
NE5534ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	5534A	Samples
NE5534ADRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	5534A	Samples
NE5534ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	5534A	Samples
NE5534AP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	NE5534AP	Samples
NE5534APE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	NE5534AP	Samples
NE5534D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	NE5534	Samples
NE5534DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	NE5534	Samples
NE5534DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	NE5534	Samples
NE5534DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	NE5534	Samples
NE5534P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	NE5534P	Samples
NE5534PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	NE5534P	Samples
SA5534AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SA5534A	Samples
SA5534ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SA5534A	Samples
SA5534ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SA5534A	Samples
SA5534AP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SA5534AP	Samples
SA5534APE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SA5534AP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SA5534D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SA5534	Samples
SA5534DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SA5534	Samples
SA5534DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SA5534	Samples
SA5534P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SA5534P	Samples
SA5534PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5534	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

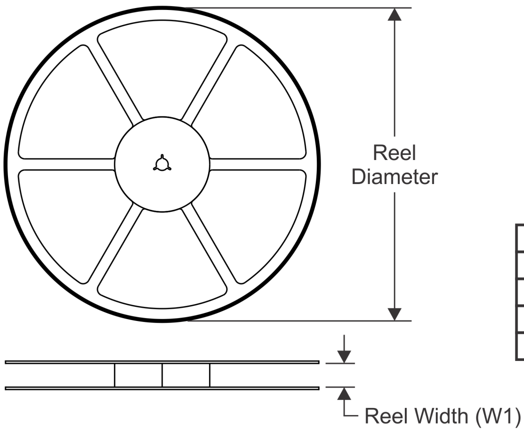
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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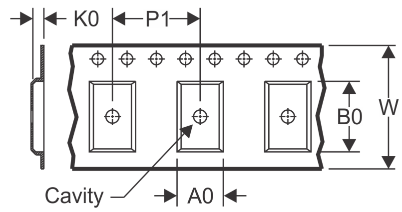
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

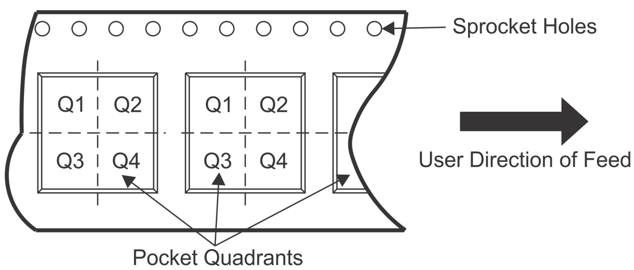


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

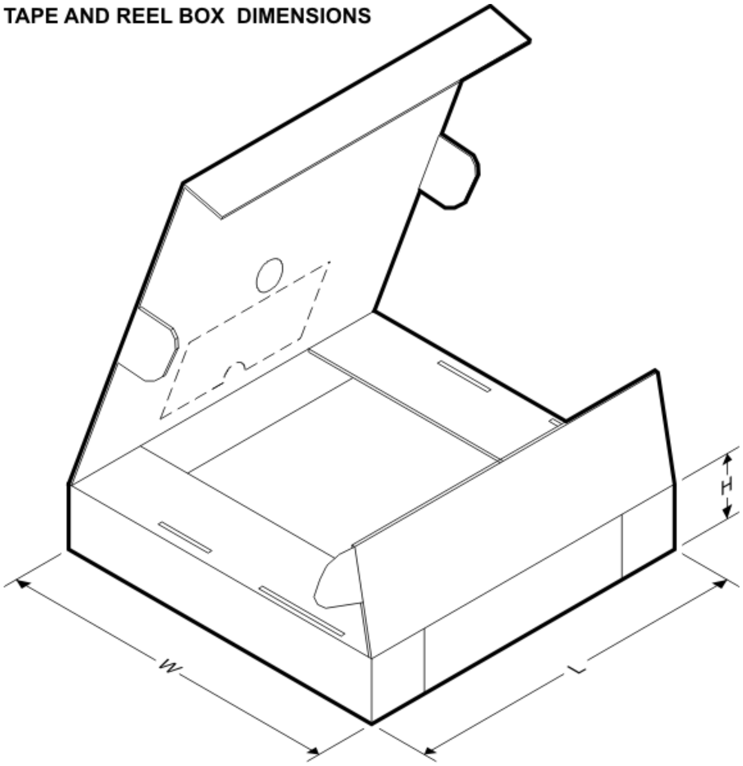
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
NE5534ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE5534DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SA5534ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SA5534DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SA5534PSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1

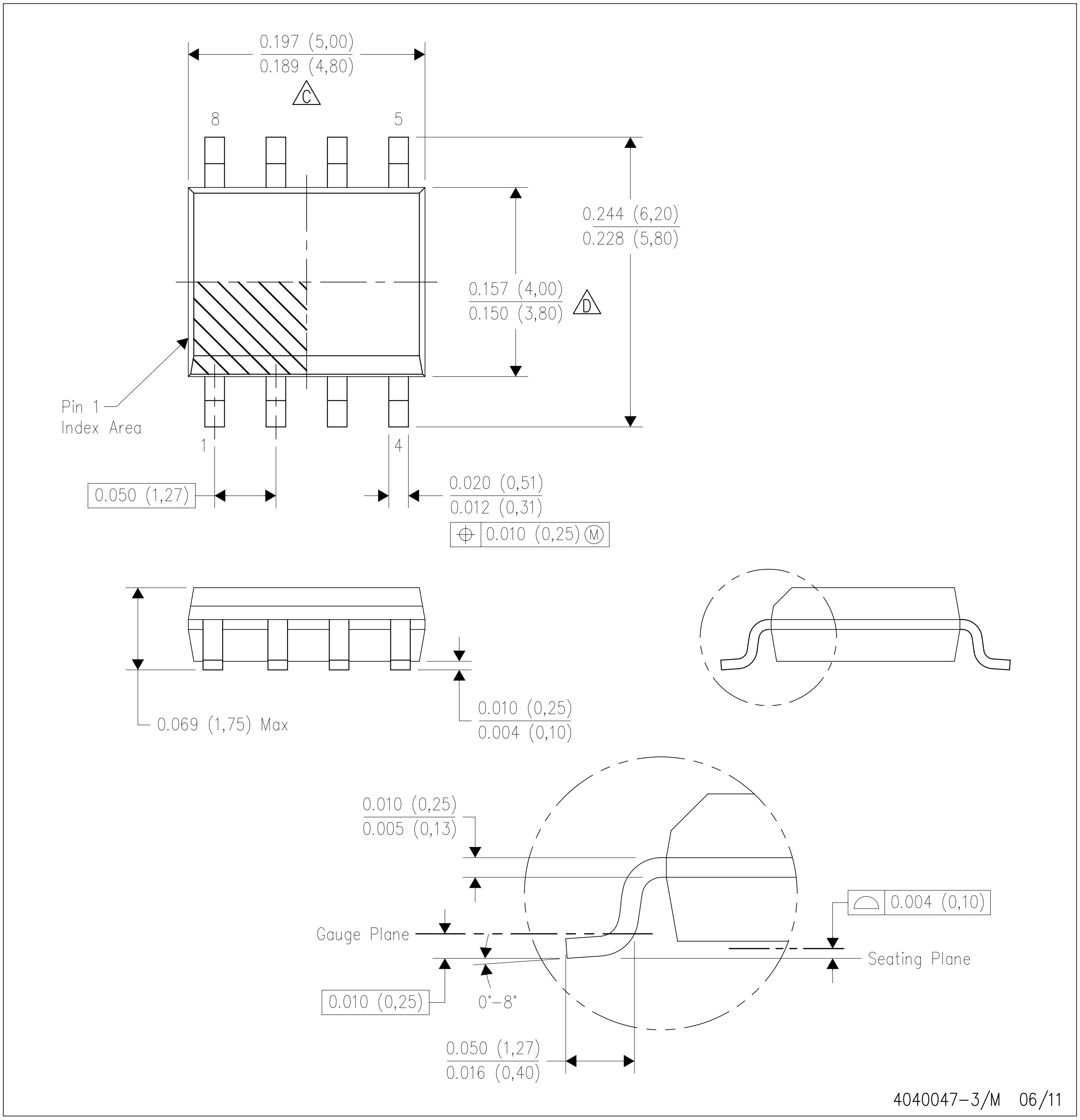
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

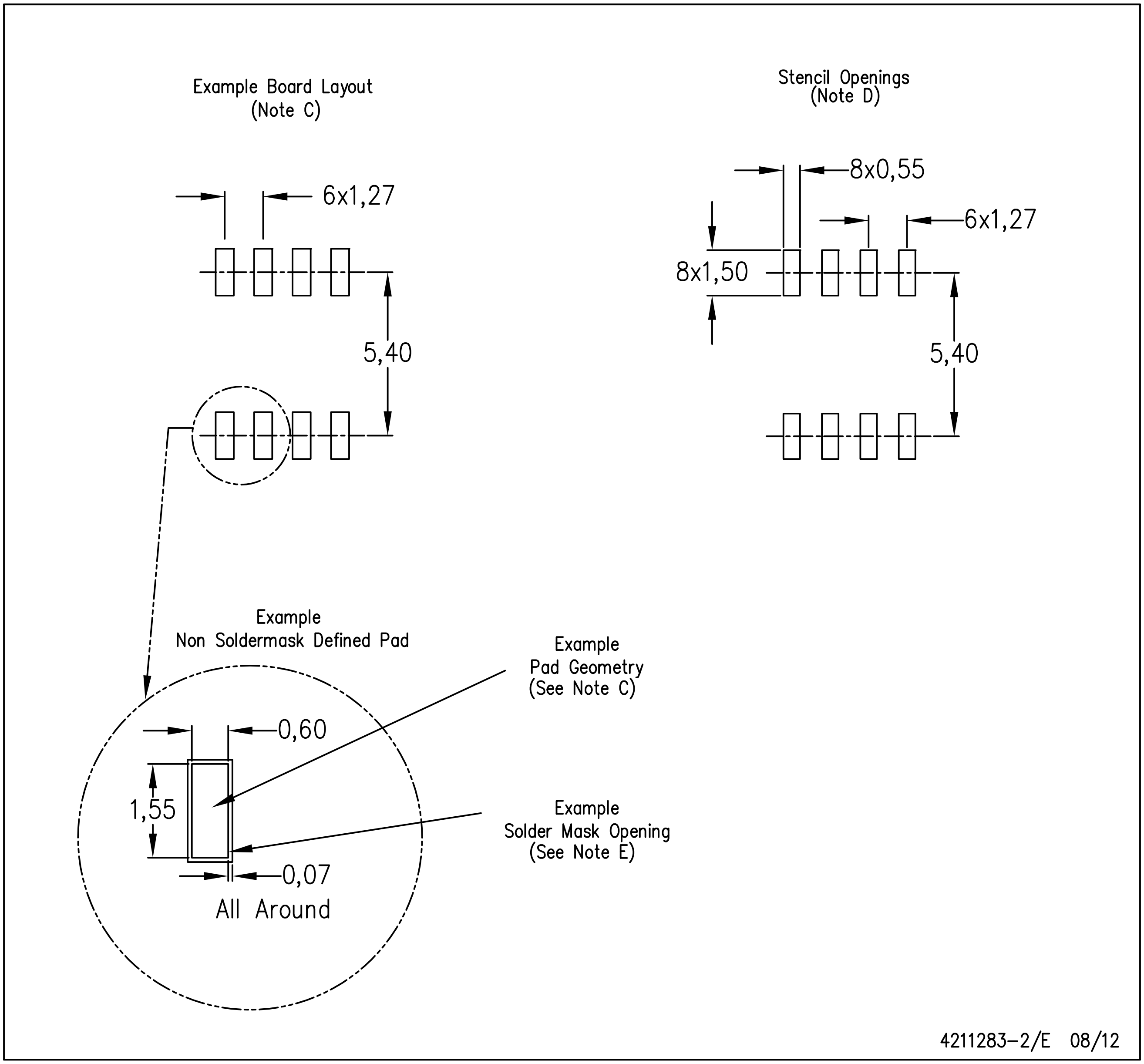
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
NE5534ADR	SOIC	D	8	2500	340.5	338.1	20.6
NE5534DR	SOIC	D	8	2500	340.5	338.1	20.6
SA5534ADR	SOIC	D	8	2500	340.5	338.1	20.6
SA5534DR	SOIC	D	8	2500	340.5	338.1	20.6
SA5534PSR	SO	PS	8	2000	367.0	367.0	38.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE

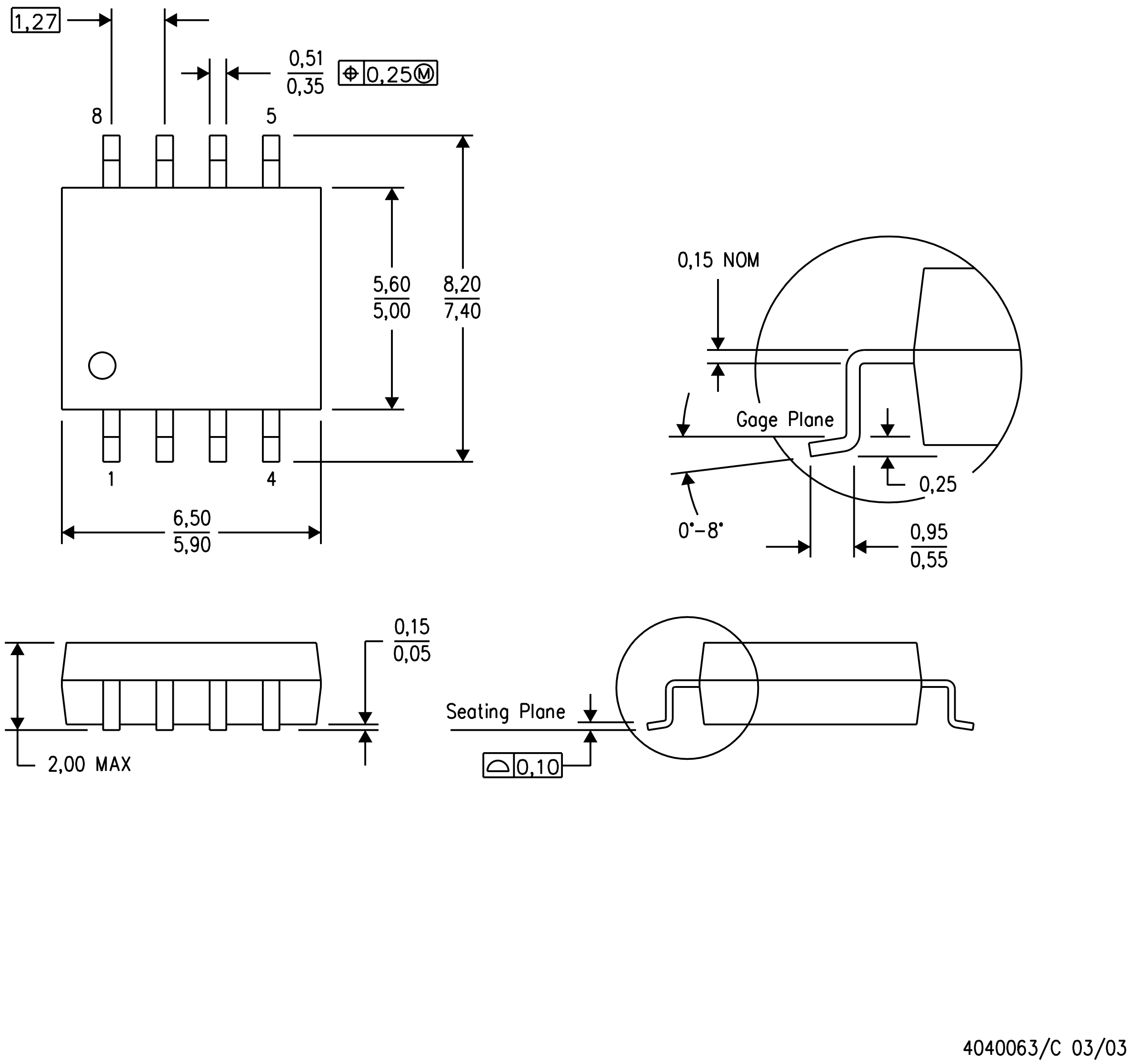


NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE

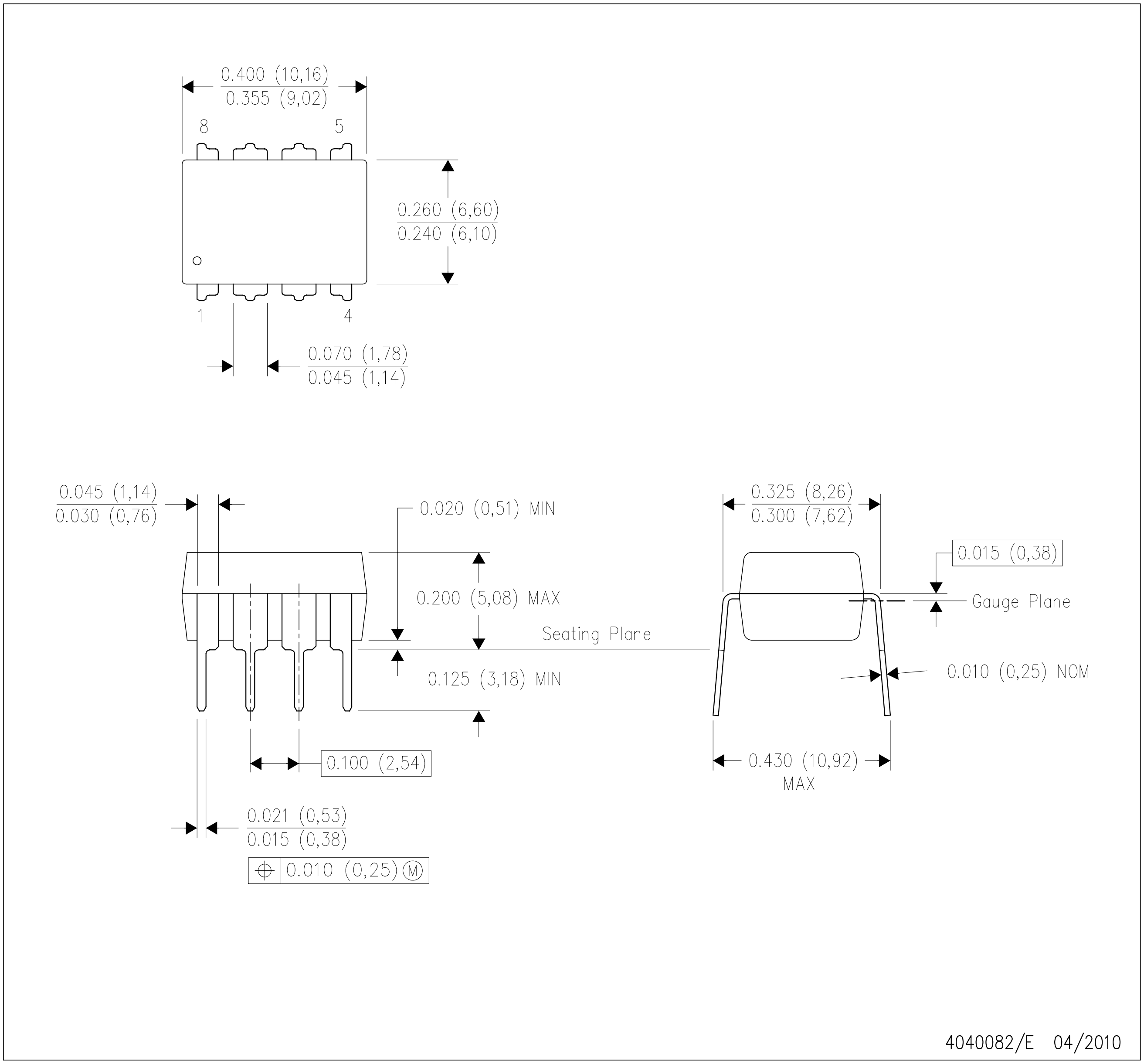


NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001 variation BA.

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